ABSTRACT

A method and apparatus are disclosed for allowing a system having multiple clock domains to be put into a known state to ensure repeatability during debugging tests. A global framing clock is created having a frequency equal to the lowest common denominator of all clocks in the system or to some divisor of thereof. At this frequency, the global framing clock ensures that it will have a rising edge at the same time that other clocks in the system have rising edges. The system clock and the global framing clock may be run throughout the system to integrated circuits. The global framing clock is used to control a system function, such as a reset or an interrupt function. When the system receives an asynchronous event, the global framing clock ensures that the event is not distributed to the system until the occurrence of a rising edge of the global framing clock. This ensures that the event will also be seen on a rising edge of every other system clock, which makes the event appear at the same time throughout the system. By ensuring that an asynchronous function, such as a reset function, appears at the same time throughout the system, the system becomes repeatable. That is, the clock states will be the same every time an asynchronous event is released to the system.